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㊴ **Erasable programmable read only memory using floating gate field effect transistors.**

㊼ For an EPROM having floating gate type FET memory cells, required marginal space allowances for mask alignment, and the incidence of bird's beaks, are cut down by applying self alignment techniques to determine both gate width and gate length.

On a substrate (1), a first gate insulation film (3) and a first conductive (e.g. polysilicon) layer (PA) are formed. Parallel grooves (11) for device separation are formed in the gate length direction by photolithography. The space between the grooves (11) defines gate width: the width of the grooves determines spacing between the cell FETs. The grooves are buried by insulator (e.g. SiO_2) (12) deposited by chemical vapour deposition. Then etching is used to expose the first conductive layer (PA), and a second gate insulation film (6) and a second conductive (e.g. polysilicon) layer (PB) are formed on the exposed surface. Parallel stripes (7) are formed, by etching the second conductive layer, orthogonal to the grooves (11). The spacing between the stripes determines device separation in the gate length direction. The stripes are then used as the mask for etching to xpose th substrate (1) in which sources (9) and drains (10) are then formed by doping

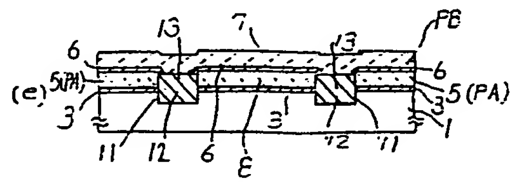
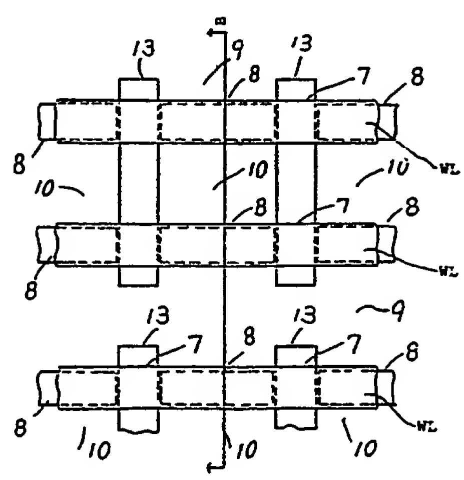


FIG. 4



(a)

FIG. 5

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Erasable programmable read only mem ry using floating gate field effect transistors

The present invention relates to erasable programmable read only memory (EPROM) using floating gate field effect transistors.

It is important to cut down on marginal space allowances in circuit patterns, in order to increase the packing density of device elements in an IC - (integrated circuit). The self alignment technique is a method which can be effectively employed for cutting down the marginal space allowances required for photolithographic mask alignment processes for fabricating ICs.

It has been proposed to apply the self alignment technique to an EPROM device composed of MOSFETs (metal-oxide-semiconductor type field effect transistors) having floating gates, to cut down the marginal space requirements on both sides of a gate (the sides between which the length of the gate of the FET is defined). However, it is still necessary to leave a margin for mask alignment in relation to processes which determine the width of a floating gate. This situation is explained briefly with reference to Figs. 1 and 2.

Fig. 1 gives plan views (a),(b),(c) schematically illustrating steps in the fabrication of an elementary memory cell of an EPROM device. Fig. 2 gives sectional views (a),(b),(c) taken along lines AA and seen in the direction indicated by arrows in the corresponding views (a),(b),(c) in Fig. 1.

As shown in Figs. 1(a) and 2(a), on a p-type silicon substrate 1, for example, a silicon dioxide - (SiO_2) film is fabricated by selective oxidation and patterned to form a matrix of islands 2 on the substrate 1, for separating device elements from one another. The islands formed of the SiO_2 film provide field oxide layer islands.

Next, as shown in Figs. 1(b) and 2(b), the entire surface of the substrate is covered with a first gate oxide film 3 of SiO_2, formed by thermal oxidation. Subsequently, the surface is covered with a first conductive polysilicon layer (PA) 5. The first polysilicon layer 5 is patterned to form stripes separated from each other by grooves 4 which are formed by etching. Each of the grooves 4 is positioned to the centre of a column of field oxide layer islands 2, so field oxide layer islands are exposed at the centre part of the groove. A stripe of polysilicon, having a width W_F, bridges between adjacent columns of field oxide layer islands 2 as shown in Fig. 1(b) The width W_F of the stripe later becomes the width of the floating gate of an FET. The direction of lines AA in Fig. 1 or the direction of the width W_F in Fig. 2 will be referred to as the gate width direction, and the orthogonal direction, namely the direction of the arrows in Fig. 1, will be referred to as the gate length direction.

Subsequently, as shown in Figs. 1(c) and 2(c), the entire surface of the substrate is covered with a second gate oxide film 6, formed by thermal oxidation.

Next, the surface is covered with a second conductive polysilicon layer (PB) 7.

Then, the second gate oxide layer 6 and the stripes of the first polysilicon layer 5 are selectively etched off leaving second stripes orthogonal to the grooves 4. The second stripes have a predetermined width W_C which later becomes the gate length of an FET.

By this etching process, portions of the first stripes 5 which are covered by the second stripes 7 become floating gates 8 of FETs, and the second stripes 7 become control gates which are extended in the gate width direction (the horizontal direction in the Figures) to become word lines. In such manner, floating gates 8 are formed underneath control gates 7 separated from the latter by second gate oxide film 6. The width and length of a floating gate 8 are respectively W_F and W_C.

The surface of the p-type silicon substrate 1 where not covered by a second stripe is then doped with n-type impurities, by ion implantation for example, to form n^+-type source 9 and drain 10 regions.

In Fig. 1(c) a floating gate 8 is shown by a broken line which gives it the appearance of being slightly narrower (shorter) than a control gate 7, in order to identify the floating gate. However, it will be understood from the above explanation that control gate and floating gate are self aligned to each other and have substantially the same width, because a floating gate 8 is etched using self alignment technique utilising a control gate 7 as mask. Therefore, there is no need to allow a marginal space for mask alignment between control gate and floating gate in the gate length direction. So, packing density of FETs in the gate length direction is increased to the limit determined by the resolution of the photolithography. However, in the orthogonal direction, the gate width direction, on the contrary, marginal space allowance is necessary.

The grooves 4 in Figs. 1 and 2 must be aligned to respective columns of field oxide layer islands 2. Since grooves 4 are formed by photolithographic etching, it is necessary, as indicated by Figs. 1(c) and 2(c), to allow a marginal space W_A on both sides of a groov 4 having a width W_S. With present state-of -the-art photolithography, marginal spaces W_A of approximately 0.3 to 0.5 μm are necessary on both sides of a groove having a width W_S of 0.6 to 1 μm for example.

Therefore, the packing d nsity of FETs in the gate width direction cannot be increased to the limit determined by the resolution of the photolithography.

Another phenomenon serving to decrease packing density in the gate width direction is th presence of invalid spaces under both sides of a floating gate, in the width W_F direction, as indicated in Fig. 2(b). These invalid spaces are identified by 111 in Fig. 2(b) and (c). They are known as "bird's beaks". They are inevitably formed on both sides - (gate width direction) of the field oxide layer islands 2. Bird's beaks extend sometimes 1 µm on both sides of a field oxide layer island 2 , and contribute neither to the conductance of the FET nor the capacitance of the floating gate.

There is an increasing need to cut down marginal space allowances and to eliminate bird's beaks, for example in the field of large scale integrated EPROMs.

Recently, an attempt to cut down marginal space allowances required for mask alignment, using a self alignment technique, has been proposed by H.Nozawa et al in "CHARACTERISTICS AND RELIABILITY OF THE SEPROM CELL" in IEEE Trans. ED vol.ED31, No.10, Oct. 1984.

Schematic diagrams illustrating the fabrication process of this proposal are shown in Fig. 3.

A first gate oxide layer 23, a first conductive polysilicon layer 25 and a silicon nitride film 31 are successively formed on a substrate 21 and the silicon nitride film 31 patterned as shown in Fig. 3(a). Then, as shown in Fig. 3(b), the first polysilicon layer 25 is oxidised to form field oxide layer 22 using silicon nitride film 31 as a mask. After removing silicon nitride film 31, a second gate oxide layer 26 is formed. Next, a second conductive polysilicon layer 27 is formed, as shown in Fig. 3(c). Then the substrate is etched in a similar manner to that illustrated in Fig. 1(c) and 2(c), and n-type impurity implanted to form n^+-type source 29 and drain 30. A cross sectional view of the device, cut along a line from source to drain, is given in Fig. 3(d).

As described above, control gate 27 and floating gate 25 are self aligned to each other. However, bird's beaks still occur. Also, as can be appreciated from the shape of Fig. 3(c), capacitance between floating gate and control gate is smaller than that between floating gate and channel region. This decreases control gate sensitivity and FET programming efficiency. Moreover, surface flatness of the device is not so good (not smooth). This can give rise to problems when forming wiring for interconnecting devices on the IC chip.

Embodiments of the present invention can provide EPROM devices having very high packing density of device lements, and can provide processes for fabricating such devices.

Embodiments of the present invention can provide a structure and a production process for an EPROM device which enables marginal space allowances on the IC chip to be cut down.

An embodiment of th present invention can provide a fabrication process for an EPROM device whose chip surface is smooth, so as to allow attainment of high reliability for interconnection wiring for device elements on the chip surface.

In an embodiment of the present invention a self alignment technique is applied in relation to gate width and gate length directions to cut down on marginal space allowances for mask alignment. A floating gate is spaced at its periphery by separation grooves formed by etching, so that no bird's beaks appear. The grooves are filled, with silicon dioxide for example, to provide a smooth chip surface.

A process embodying the present invention for fabricating an EPROM device comprises the following main steps:

(a) forming successively a first gate insulation film and a first conductive layer on a substrate;

(b) forming separation grooves, arranged parallel to each other and extending in the gate length direction of memory cell FETs to be fabricated on the substrate. The space between the separation grooves is equal to the gate width of the memory cell FETs, and the depth of the grooves is such that they penetrate through the first conductive layer and the first gate insulation film to dig into the substrate;

(c) forming a thick insulation layer over the substrate to bury (fill) the separation grooves formed in step (b);

(d) etching off the thick insulation layer formed in step (c) to expose the surface of the first conductive layer;

(e) forming a second gate insulation film over the surface (of the first conductive layer and insulation remaining in the grooves) exposed in step (d), and subsequently forming a second conductive layer over the entire surface of the substrate;

(f) etching off the second gate insulation film leaving parallel stripes arranged to extend orthogonally with respect to the first separation grooves. The spaces between the stripes are equal to the spaces between memory cell FETs to be fabricated on the substrate, and the width of the stripes is equal to the gate length of the memory cell FETs. Then, etching off the second gate insulation film, the first conductive layer and the first gate insulation film to expose the substrate;

(g) implanting impurities into the exposed substrate to form sources and drains of the memory cell FETs

The etching processes in steps (b) and (f) are self aligned etching processes. Therefore, marginal space allowances for the lithography are unnecessary. Further, the memory cell FETs are separated by insulation layers buried in the separation grooves, so no bird's beaks appear.

The packing density of the memory cell FETs can thus be increased to the limit of photolithographic resolution.

Reference is made, by way of example, to the accompanying schematic drawings, in which:

Fig. 1 gives plan views (a),(b),(c) illustrating steps in the fabrication of an elementary memory cell of an EPROM device;

Fig. 2 gives sectional views (a),(b),(c) taken along lines AA and seen in the direction of the arrows in the corresponding views (a),(b),(c) of Fig. 1;

Fig. 3 gives sectional views (a) to (d) illustrating a process in which a self alignment technique is applied to the fabrication of a floating gate FET;

Fig. 4 gives sectional views (a) to (e) illustrating schematically steps in a fabrication process in accordance with an embodiment of the present invention; and

Fig. 5 gives a partial plan view (a) and a cross sectional view (b), taken along line BB and seen in the direction of the arrows in view (a), illustrating schematically the structure of an EPROM memory cell in an EPROM device embodying the present invention.

The configuration of an EPROM memory cell provided by an embodiment of the present invention and a fabrication process embodying the present invention will be described with reference to Figs. 4 and 5.

First, as shown in Fig. 4(a), a first gate oxide film 3 of silicon dioxide , having a thickness of 50 to 500 Angstroms, is formed by ordinary thermal oxidation on a p-type silicon substrate 1, having a resistivity of 10 to 20 Ohm cm for example. The entire surface of the substrate is then coated with a first conductive layer PA of polysilicon having a thickness of 3000 to 4000 Angstroms. This first polysilicon layer PA is formed by chemical vapour deposition (CVD), and is doped, with phosphorus or arsenic for example, so as to be conductive. The doping is carried out by conventional gas diffusion or ion implantation for example, during or after growth of the polysilicon PA.

Next, as shown in Fig. 4(b), the first polysilicon layer PA is grooved with a plurality of parallel device separation grooves 11. Each of the grooves has a width dF of 1μm and a depth of 0.6 μm for example. The depth of the grooves is not so critical. In the Figure, the grooves 11 penetrate through the first polysilicon layer PA and the first gate oxide film 3 and they reach to the substrate 1, penetrating it to a depth of 2000 to 4000 Angstroms. These grooves 11 are formed using a photolithographic mask and conventional reactive ion etching (RIE). Th grooves 11 are separated from each other by a distance W_F which later becomes the gate width of memory cell FETs. Though the distance W_F appears rather large in the Figure, it corresponds to a gate width W_F of 1 μm.

Then, as shown in Fig. 4(c), a silicon dioxide layer 12 0.5 to 1 μm thick is formed on the entire surface of the substrate. So, the grooves 11 are perfectly buried by SiO_2. Before forming the SiO_2 layer 12, it is desirable to cover the entire surface of the substrate by a thermal oxidized thin SiO_2 film 12′ a few hundred Angstroms thick. This SiO_2 film 12′ protects edges of parts of the polysilicon layer PA, which later become memory cell FET floating gates, from contamination which might be included in the CVD grown thick SiO_2 layer 12, and prevents leakage current. However, since the thin SiO_2 layer 12′ and the thick SiO_2 layer 12 are both silicon dioxide, and they cannot be distinguished from each other, in the following Figures separate indication of the thin SiO_2 film 12′ is omitted.

Next, as shown in Fig. 4(d), the surface of the substrate is polished until the surface of the polysilicon layer PA is exposed. The polishing may be mechanical, but it is preferred to use reactive ion etching (RIE) using fluoroform (CHF_3) as an etchant gas to etch off the SiO_2 layer 12 to provide a flat etched surface. It is easy to stop the polishing or etching of the substrate, watching the surface for exposure of the first polysilicon layer PA. If RIE as described above is applied, SiO_2 is etched faster than the polysilicon so, precisely speaking, the surface of the buried SiO_2 12 is slightly over-etched with respect to the surface of the first polysilicon layer PA, as can be seen in Fig. 4(d). However, the level difference between the surface of the first polysilicon layer PA and SiO_2 12 in the groove is negligibly small, so a flat surface is obtained.

Later, SiO_2 12 in a groove 11 becomes a device separation region 13 buried in the substrate, and the width dF of the buried SiO_2 12 becomes the device separation width W_{IF} between memory cell FETs. It will be noted that the photolithographic mask is used only once in the step of Fig. 4(b), and the device separation regions are formed by self alignment, therefore, the device separation width W_{IF} is equal to dF the width of the groove 11. There is no marginal space allowance for mask alignment on the two sides of the gate width W_F. Further, since the separation regions 13 are formed by etching, there appear no bird's beaks.

Next, as shown in Fig. 4(e), the surface of the first polysilicon layer PA is covered with second gate oxide film 6, 300 to 500 Angstroms thick, fabricated by thermal oxidation. Then, over the ntire surface of the substrate, a second polysilicon lay r PB, 4000 to 4500 Angstroms thick is formed. The second polysilicon layer PB is deposited by CVD, and is doped with phosphorus or arsenic during or after its growth, by gas diffusion or ion implantation for example.

Then, the second polysilicon layer PB is patterned by photolithography to form parallel stripes oriented orthogonally with respect to the device separation grooves 11. The width of a stripe later becomes the gate length of a memory cell FET, and the spacing between the stripes becomes the spacing between memory cells in the gate length direction. For example, the width of a stripe is 1 μm, and the spacing between stripes is 1.2 to 1.5 μm. Each of the stripes becomes a control gate electrode 7 which extends on both sides of the Figure to form a word line WL as shown in Fig. 5. Utilising this control gate electrode 7 as a mask, the second gate oxide film 6, first polysilicon layer PA and first gate oxide film 3 are etched off successively to expose the surface of the p-type silicon substrate.

By this etching process, floating gates 8 of the memory cell FETs are formed underneath the gate electrodes 7. The floating gates 8 are insulated from the substrate 1 and the gate electrode 7 respectively by the first and second gate oxide films 3 and 6. It will be understood that the floating gates 8 and the control gates 7 are self aligned, so there is no marginal space allowance for photolithography in the gate length direction. Further there appear no bird's beaks since the device separation regions 13 are formed by etching. Thus, marginal space allowances and the occurrence of bird's beaks in both gate length and gate width directions are cut down.

At this stage, it is desirable, as shown in Fig 5-(b), to form a thin SiO_2 film 12", a few hundred Angstroms thick, on both sides of the floating gates 8 and the control gates 7 to protect them from contamination. Fig. 5(b) is a cross sectional view of the device of Fig. 5(a) taken along line BB and seen in the direction of the arrows.

n^+-type impurities such as arsenic for example, are doped into the exposed surface of the substrate 1 to form sources 9 and drains 10 as shown in Fig. 5. The doping may be effected by ordinary means such as diffusion or ion implantation. If it is effected by a diffusion process, the thin SiO_2 film 12" on the surface of th substrate should be removed beforehand. It may be left in place if the doping is effected by ion implantation.

As can be seen in Fig. 5, device separation regions 13 are not extended continuously in the gate length direction, but are interrupted at source regions 9. This is a modification of the above described processes and is provided due to the fact that, in EPROM d vices, the source regions should be connected to each other in the direction of a word line WL. It will be readily understood that such interruption of the device separation regions can be effected by interrupting the device separation grooves 11 at the stage of Fig. 4(b). By providing such interruptions of regions 13, interconnection wiring for connecting sources is saved.

In such manner, the main parts of EPROM memory cell FETs are fabricated. Subsequently, the FETs are interconnected on the surface of the substrate. Though it is not shown in the Figures, the surface of the device is coated with a passivation layer of phosphosilicate glass (PSG) for example, and contact windows are opened to contact to the drains 10, for example. Then, interconnection wiring, such as bit lines for example, is provided through these contact windows, and the device is completed.

Applying an embodiment of the present invention to an EPROM device, the packing density of memory cells has been increased by 30% as compared with that of a previously proposed device.

In the above description reference is made to a p-type silicon substrate. It will be clear, however, that embodiments of the present invention can be applied to n-type substrates merely by varying the conductivity types of impurity materials. The first and second polysilicon layers PA and PB may be replaced by other kinds of conductive material, such as metal silicide. The semiconductor material used is not limited to silicon. Embodiments of the present invention may be applied to other kinds semiconductor materials, such as gallium arsenide for example.

For an EPROM having floating gate type FET memory cells, required marginal space allowances for mask alignment, and the incidence of bird's beaks, are cut down by applying self alignment techniques to determine both gate width and gate length.

On a substrate (1), a first gate insulation film -(3) and a first conductive (e.g. polysilicon) layer -(PA) are formed. Parallel grooves (11) for device separation are formed in the gate length direction by photolithography. The space between the grooves (11) defines gate width: the width of the grooves determines spacing between the cell FETs. The grooves are buried by insulator (e.g. SiO_2) (12) deposited by chemical vapour deposition. Then etching is used to expose the first conductive lay r (PA), and a second gate insulation film (6) and a second conductive (e.g. polysilicon)

layer (PB) are formed on the exposed surface. Parallel stripes (7) are formed, by etching the second conductiv layer, orthogonal to th grooves - (11). The spacing between the stripes determines device separation in the gate length direction. The stripes are then used as the mask for etching to expose the substrate (1) in which sources (9) and drains (10) are then formed by doping.

Claims

1. An erasable programmable read only memory (EPROM) having a plurality of memory cell field effect transistors (FETs) arranged in a matrix on a semiconductor substrate (1), each memory cell FET comprising:

a floating gate (8), for storing voltage thereon and controlling the conductivity of the memory cell FET;

a first gate insulation film (3), provided between the floating gate and the substrate for insulating the floating gate from the from the substrate;

a control gate (7) positioned over the floating gate, for controlling the voltage of the floating gate;

a second insulation film (6) provided between the floating gate and the control gate, for insulating the floating gate from the control gate; and

device separation regions (13) provided on both sides of the floating gate in the gate width direction, for separating the memory cell FET from adjacent memory cell FETs an both those sides,

wherein the floating gate is positioned underneath the control gate, the width of the control gate being equal to the length of the floating gate, and the floating gate and device separation regions being aligned side by side at the edges of the floating gate on its gate width sides.

2. An EPROM as claimed in claim 1, wherein each memory cell FET further comprises a thin insulation film (12") covering side edges of the floating gate (8) and the control gate (7).

3. An EPROM as claimed in claim 1 or 2, wherein the floating gate (8) and the control gate - (7) are of polysilicon.

4. An EPROM as claimed in claim 1, 2 or 3, wherein the substrate (1) is of silicon, the first gate insulation film (3), the second gate insulation film - (6), and the thin insulation film (12") are of silicon dioxide.

5. An EPROM as claimed in claim 1 or 2, wherein the floating gate (8) and the control gate - (7) are of metal silicide.

6. A process for fabricating an erasable programmable read only memory (EPROM) having a plurality of memory cell field effect transistors - (FETs) arranged in a matrix on a semiconductor substrate, th process comprising:

(a) forming successively on a semiconductor substrate (1), having a first conductivity type, a first gate insulating film (3) and a first conductive layer - (PA,5);

(b) forming by photolithography a plurality of parallel device separation grooves (11) extending in the gate length direction of the memory cell FETs to be fabricated, the spacing between the device separation grooves (11) being equal to the gate width of the memory cell FETs to be fabricated, and the depth of the grooves (11) being such that they penetrate through the first conductive layer and the first gate insulation film into the substrate - (1);

(c) forming a thick insulation layer (12) to bury the device separation grooves;

(d) removing parts of the thick insulation layer to expose the surface of the first conductive layer;

(e) forming a second gate insulation film (6) over the exposed surface of the first conductive layer and subsequently forming a second conductive layer (PB,7) thereover;

(f) etching off the second conductive layer to leave parallel stripes (7) of the material of that layer arranged orthogonally of the device separation grooves, the spacing between the stripes being equal to the spacing between the memory cell FETs to be fabricated, and the width of the stripes being equal to the gate length of the memory cell FETs to be fabricated, and then etching off successively the second gate insulating film, the first conductive layer and the first gate insulation film to expose the semiconductor substrate, using the parallel stripes (7) as a mask; and

(g) doping impurities, having conductivity type opposite to that of the semiconductor substrate, into the exposed semiconductor substrate to form source (9) and drain regions (10) of the memory cell FETs to be fabricated.

7. A process as claimed in claim 6, further comprising:

(b') between steps (b) and (c), forming a thin insulation film (12') over the surface exposed at the conclusion of step (b);

(f') between steps (f) and (g), forming a thin insulation film (12") over the surface exposed at the conclusion of step (f).

8. A process as claimed in claim 6 or 7, wherein the substrate (1) is of silicon, and the first gate insulation film (3) and the second gate insulation film (6), and the thin insulation films (12',12") where provided, are of silicon dioxide, formed by thermal oxidation.

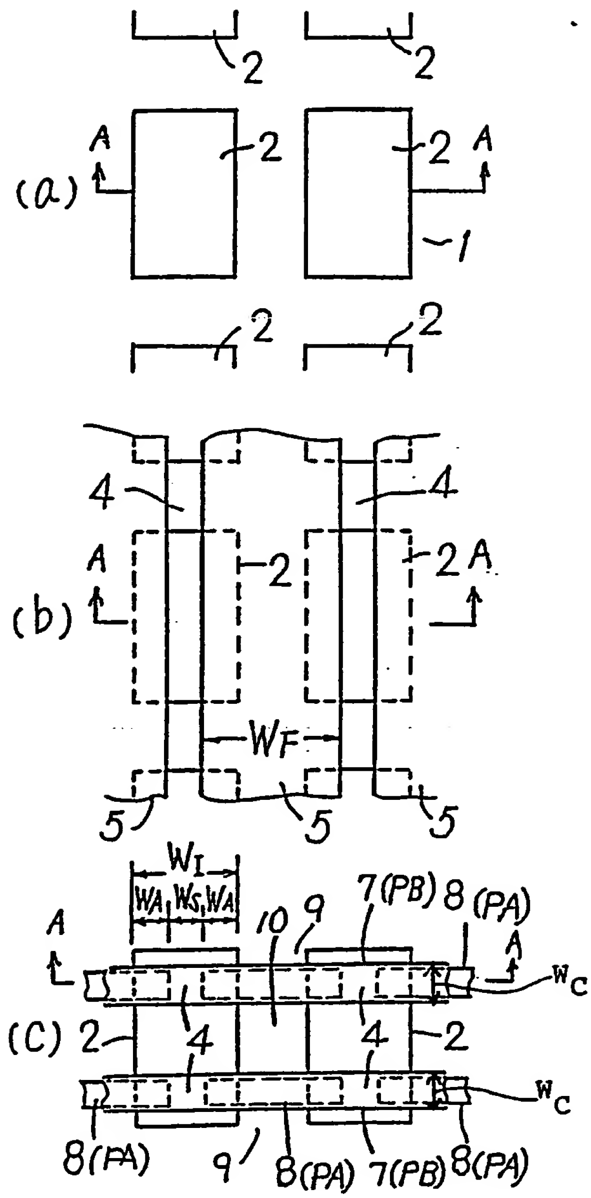
9. A process as claimed in claim 6, 7 or 8, wherein the first (PA,5) and second (PB,7) conductive layers are of polysilicon formed by chemical vapour deposition.

10. A process as claimed in claim 6, 7, 8 or 9, wherein step (d) is accomplished by reactive ion tching.

11. A process as claimed in claim 6, 7, 8 or 9, wherein step (d) is accomplished by mechanical polishing.

12. A process as claimed in claim 6, 7, 8, 9 or 10, wherein the etching processes employed in steps (b) and (f) are reactive ion etching processes.

13. A process as claimed in any one of claims 6 to 12, wherein step (c) is a chemical vapour deposition process and the thick insulation layer is a silicon dioxide layer.


(a)
A
A
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(b)
4
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WI
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9
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WC
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7(PB)

FIG. 1

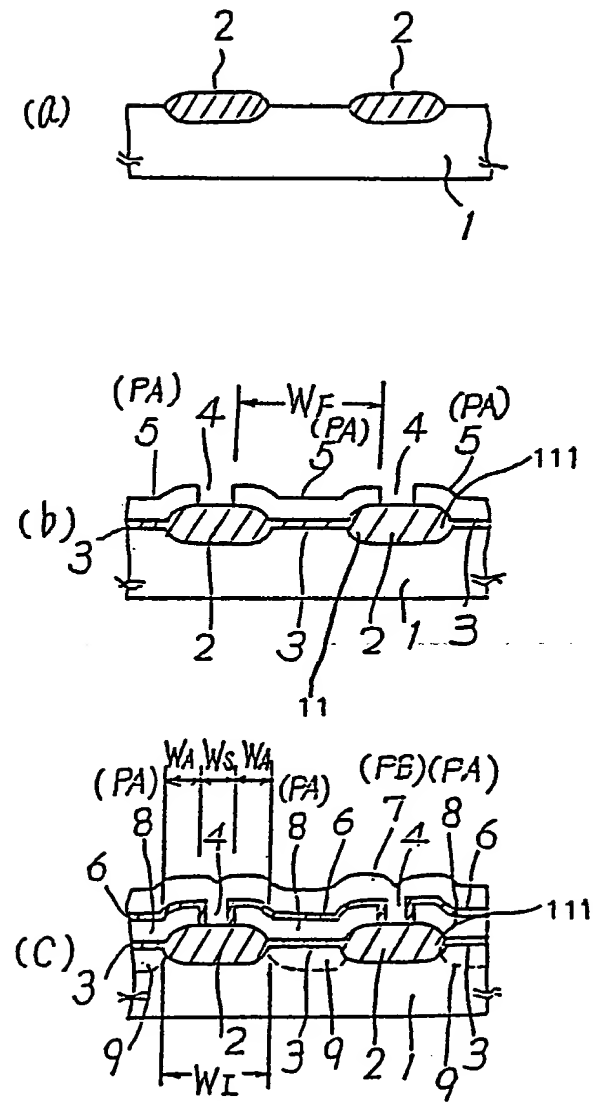
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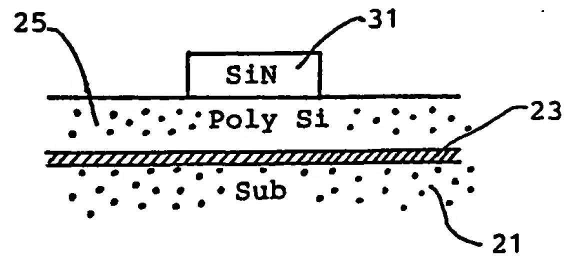
FIG. 2

(a)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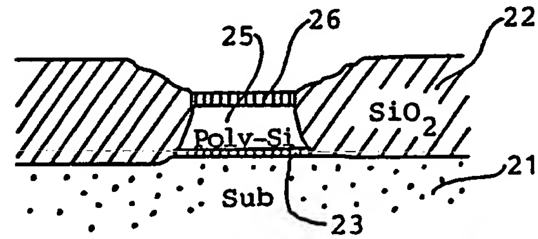
21

(b)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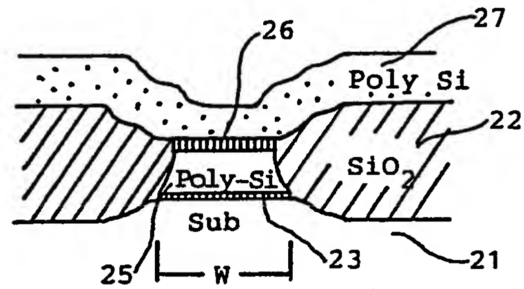
23

(c)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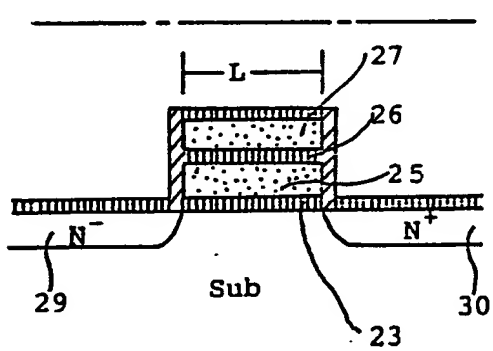
(d)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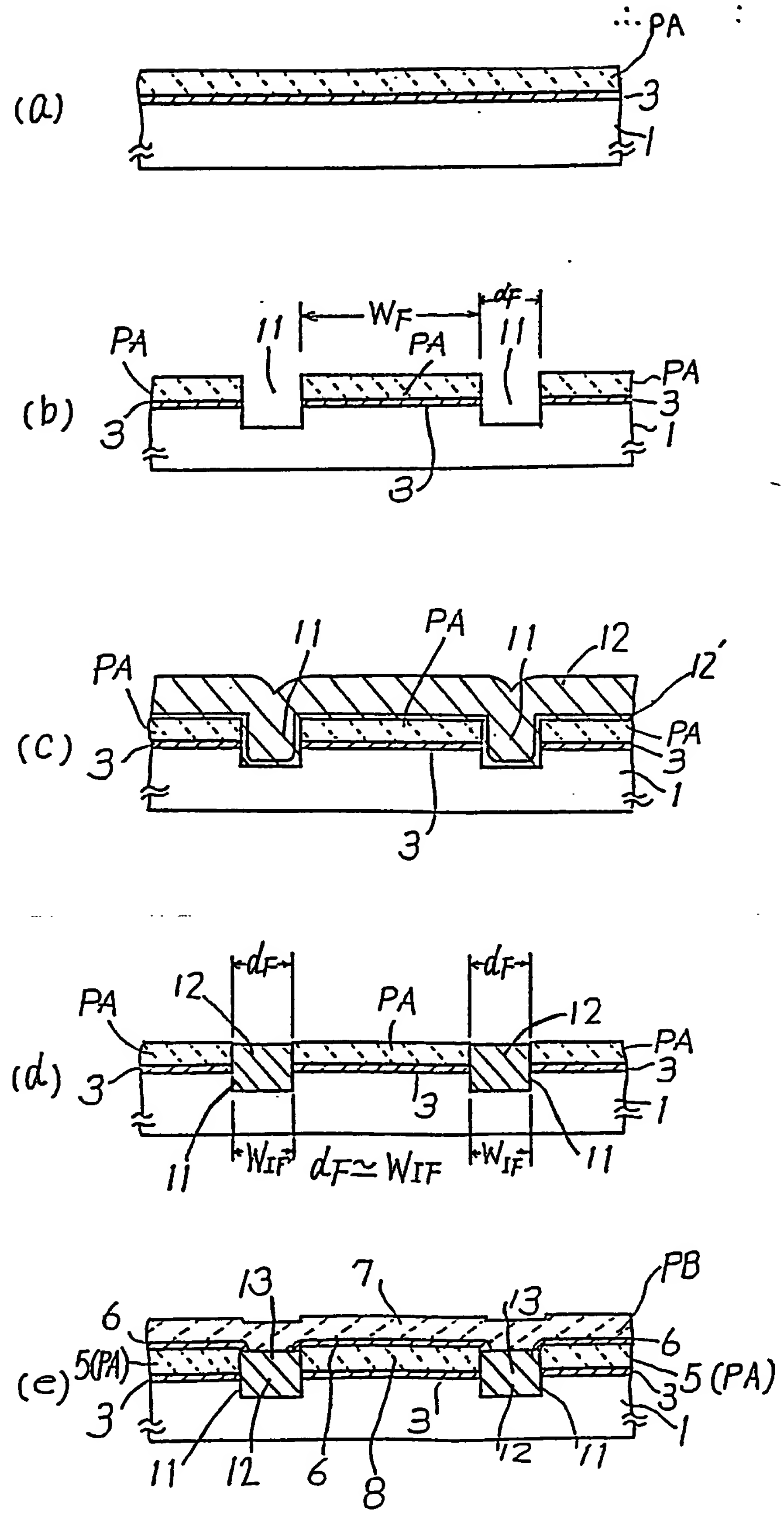
N+
29
Sub
30
23

FIG. 3



PA
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PA
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d_F
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PA
(b)
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3
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PA
11
12
PA
12'
(c)
3
PA
3
1
3
d_F
d_F
PA
12
PA
12
PA
(d)
3
3
3
1
11
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$d_F \simeq W_{IF}$
W_{IF}
11
13
7
PB
6
13
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5 (PA)
(e)
3
3
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3
1
11
12
6
8
12
11

FIG. 4

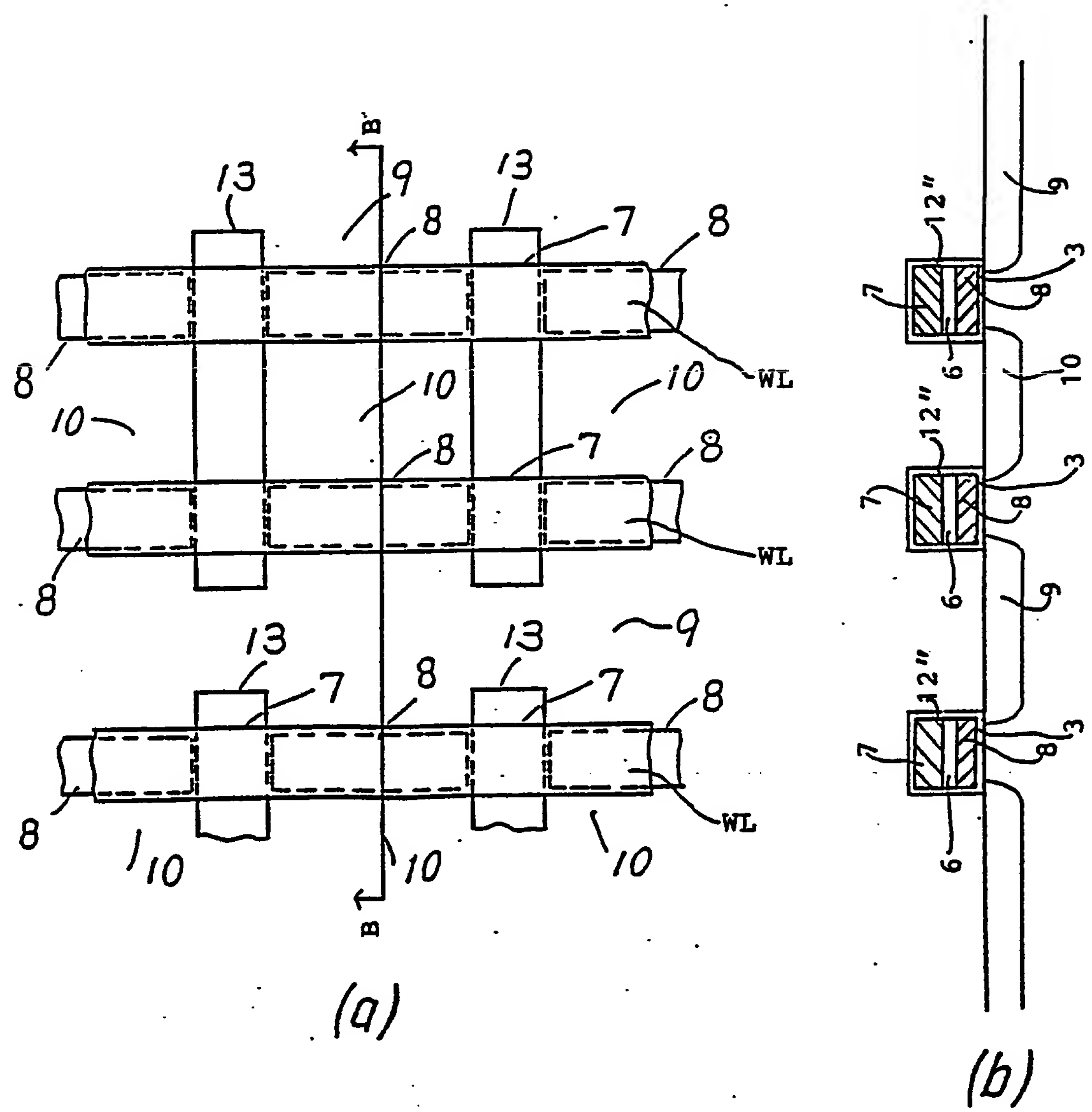

FIG. 5